技術報告

次世代半導体材料開発の取り組み：22nm 世代以降の CMOS デバイス向け低温シリコンエピタキシャルプロセスの開発

Challenges for next generation semiconductor material development: Low temperature silicon epitaxial process development for 22nm node and beyond CMOS

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シリコンベースの低温（<600°C）エピタキシャル成膜プロセスは，22nm ノード以降の CMOS デバイスのソースドレイン形成にとって，非常に重要な技術となっている。我々は，低温プロセスと量産性の両方を実現するため，シリコン原料として TF-2 の開発を実施している。本報告では，デバイスメーカーと共同で行っている次世代の CMOS 向けリセスソースドレイン用エピタキシャル成膜の開発の取り組みについて報告する。

Low temperature (<600°C) silicon-based epitaxial growth process is a key technology for Source/Drain formation of CMOS device for 22nm node and beyond. We are developing TF-2 unique silicon precursor for both low temperature process and high volume manufacturing. In this report, we present the challenges for epitaxy for recess source drain of next generation CMOS device.

1. Introduction

Low temperature silicon-based strained epitaxial process is required for 22 nm-node Complimentary Metal Oxide Semiconductor (CMOS) technology applications. For CMOS stressors films for both nMOS and pMOS applications, epitaxial growth conditions are chosen to allow the maximum amount of substitutional C and metastable Ge in each film respectively. Specifically, low temperatures are required for high C & Ge % in Si. These low temperature processes also allow incorporation of dopants far above solid solubility limits.

High boron concentration (3-6x10^{20} atoms cm^{-3}) and high Ge fraction (40-60%) pseudomorphic SiGeB layers are desirable for future P type MOS technology for device performance enhancement via source/drain stressors. For the pMOS process, the Selective Epitaxial Growth (SEG) of SiGeB has been deposited with traditional Si precursors such as Dichlorosilane (DCS) and silane in the recent past. HCl has been used with these precursors as a co-flow etchant and the deposition temperature has been > 600°C to enable selective growth [1]. Cyclical Deposition and Etch (CDE) has also recently been used at elevated temperatures with silane chemistry with some success but high Ge fractions can not be achieved at these conditions (>650°C). We have developed a unique high order silane precursor (code name: TF-2) based CDE 500°C isothermal process for SiGeB processes for stressor pMOS films up to ~40% SiGe ~60nm thick. Based on the SiGe critical thickness curves, there is a requirement for a 500°C process for a 60nm thick 40% and higher SiGe layer. Only high order silanes such as TF-2 can meet the materials and throughput requirements at such low temperatures.

For N type MOS technology, highly Phos-doped (3-5x10^{20} atoms cm^{-3}) pseudomorphic meta-stable Si:C layers with fully substitutional C levels in excess of 2 % are desired. In order to achieve such high carbon fractions, high-growth rates and low temperatures (<600°C) are required. For the nMOS process, the SiCP film has been deposited with disilane (growth rate: 17nm/min) in the literature[2].

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The maximum amount of substitutional C with disilane is approximately 1.5% based on a deposition temperature 625°C. To reach the goals of our development up to 2.5% substitutional C is required. To enable this processing temperatures as low at 550 °C are needed with high growth rates. High growth rates at very low temperature in Si CVD epitaxy result in high impingement rates allowing maximum Csub and P-doping. TF-2 meets the requirements for a Si precursor at this temperature.

2. Moisture challenges of low temperature growth process

2.1 Moisture behavior at low temperature

The very low deposition temperatures required to keep the C in the lattice sites of SiCP films and SiGeB peudomorphically strained imposes severe challenges in epitaxy. **Fig. 1** depicts the reversible reaction of water and Si surface at different temperatures versus partial pressure of moisture [3].

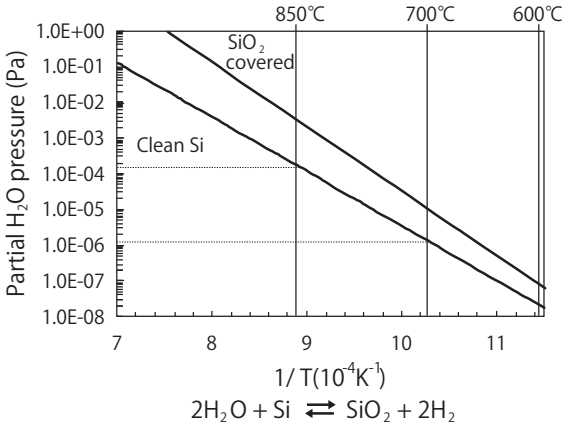

Fig. 1: Formation of SiO_2 as a function of H_2O partial pressure and temperature: reconstructed from reference [3]

Since water is the most persistent contaminate in any vacuum deposition system it can causes serious issue for epitaxy. Epitaxy requires atomically clean surfaces without SiO or SiO_2 bonds. As can be shown from this graph, every 100°C the temperature is lowered the critical partial pressure requirement for moisture becomes orders magnitude more stringent. For example, to maintain oxide free surfaces at 600°C the partial pressures for water must be below $1x10^{-7}$ Pa. In our standard Reduced Pressure Chemical Vapor Deposition (RPCVD) epi system, standard dry pumps are utilized. The base pressure in these pumps is approximately $1x10^{-1}$ Pa. The challenge then is how to produce partial pressures for water in the $1x10^{-7}$ Pa range when you have a $1x10^{-1}$ Pa base pressure with a dry pump. This is a daunting task but can be achieved.

2.2 Gas purification

These low water pressures required by low temperature epitaxy for deposition of SiCP and SiGeB films are made possible by ultra-gas purification. **Fig. 2** shows some of the equipment that makes the low partial pressures for water possible. The purification is utilized on the House (H_2, N_2 and He) to lower moisture to <100 ppt, and less than 10 ppb on most specialty gases. For HCl purification, cold trap technology is used to remove moisture to less than 10ppb. An analytical test station consisting of 4 different analytical techniques for oxygen/moisture detection is capable of sampling from before or after the RPCVD tool. Liquid precursors for Si, C and dopant to the system are supplied to the tool via the bubbler. These liquid precursors are purified to ~ 1 ppm for moisture.

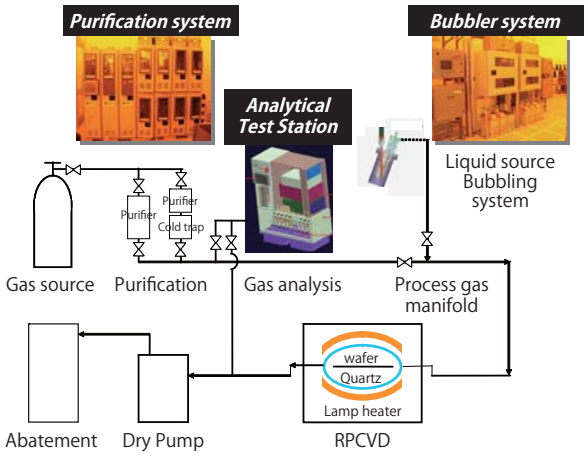

Fig. 2: The system of gas purification and gas delivery

3. Low temperature H_2 prebakes for epitaxy

Thermal budget is a major concern for all future generation CMOS 22nm and beyond devices. For Si heteroepitxial films consisting of SiCP and SiGeB for CMOS stressors on SOI, the thermal budget for the H_2 pre-bake should be kept at 800°C or below to prevent Si migration and agglomeration. Reducing thermal budgets reliably and repeatably to less than 800°C has proven to be difficult to achieve especially with potentially long queue times in the manufacturing Fab between the HF last wet clean and the onset of the epitaxial deposition.

Wet and dry clean of the silicon surface are used to remove native oxide from the surface. However, there are still residual impurities that require desorption via thermal baking to provide a clean interface. This thermal baking leads to unwanted increase of thermal budget. The greater the surface impurities concentration the longer and higher the

temperature required for removal of these impurities. In production line environment, long queue times (>24 hours) are typical. During these queue times, impurities rebuild up on the surface after the initial wet clean. The combination of ultra-high purity gases and low-pressures during thermal bakes can be used to minimize thermal bake temperatures.

We have found a non-surface technique has been found to reliably quantify the remnant interfacial sub-oxide after various wet cleans and dry cleans, and thereby minimize thermal budget in the H_2 pre-bake step. This technique is also applied to evaluating the interface after different length queue times that might be encountered in the typical manufacturing area. **Fig.3** shows the technique being used to evaluate 4 different commercial wet/dry cleans at Albany NanoTech (ANT) [4].

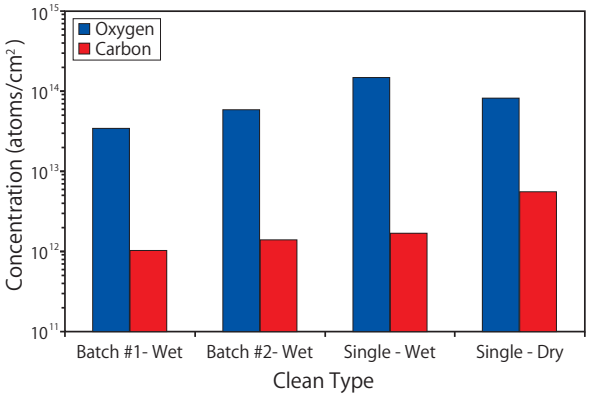

Fig. 3: Interface doses for Carbon and Oxgen atom after Wet & Dry cleans, no pre-bake, cold load, with 150nm Si deposition at 650℃ (2hours queue time)

By identifying the commercial clean that repeatably delivers the lowest initial O area density it is possible to lower the Epitaxial H_2 pre-bake temperature approximately 75°C from the standard IBM ANT pre-bake of 850°C. Queue times up to 2 hours yield no interfacial O at 775°C as shown in **Fig.4** SIMS depth profile.

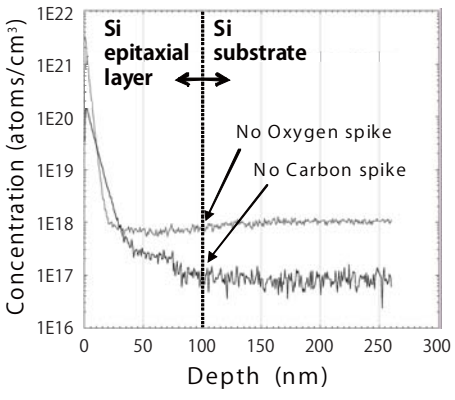

Fig. 4: SIMS depth profile with proper wet clean and minimized temperature (775℃) H_2 pre-bakes for epitaxy

4. Process optimization for TF-2 precursor

4.1 Cyclical deposition and etch process

4.1.1 Selective growth

Normal SEG processes with traditional Si precursors such as DCS and silane are co-flow processes. Co-flow means that the Si source and the etchant are flowed at the same time to achieve selectivity. Selectivity is achieved by delaying or eliminating the nucleation of growth on the dielectric areas of the patterned wafers. Co-flow SEG processes are normally achieved with either HCl or Cl_2 as an etchant so processing under 600°C becomes very difficult due to limited etching in this temperature regime. The higher silanes, such as trisilane and TF-2, are almost impossible to make selective in a co-flow fashion due to the sticking co-efficient of these precursors of approximately 1. Therefore, it is necessary to deposit them in a blanket fashion (non-selective) and then do an etch back to achieve selective growth (See **Fig.5**).

4.1.2 Crystallographic-corner defect

It is now known that crystallographic defects arise from the growth of Si:C on bare (110) substrates [5]. Si/ SiGe films deposited on these bare (110) substrates yield perfect defect free films. When XRD measurements (measuring only substitutional C) are made of Si:C films deposited on (110) substrates no C is detected. When SIMS (measuring total C) is done on these same films % level C is present. This indicates that the C on the (110) is completely interstitial or Si:C precipitate. When a recess is formed in the (100) material with the patterning normal to the notch the recess sidewalls are then (110) plane. This is the normal case for device makers. Growth of Si:C/ SiCP epi proceeds normally on the exposed bottom of recess (100) and micro-twinning occurs on the exposed sides. If a one step deposit is attempted the micro-twinning is so severe it occupies the entire sidewall and appears to be nearly poly by appearance although TEM verifies it is heavily defective crystalline material. The standard deposit time of the TF-2 SiCP process is 7 seconds. The deposit time is critical in elimination the defects. Only about 4nm of growth on Si and dielectric occurs during this short time period. It would be beneficial for throughput to increase the deposit time, but increasing it only by 1-2 seconds results in micro-twins which can't be removed by the subsequent etch. Although high amorphous etch rates are obtained with the CDE etch (200nm/min) the micro-twin region is

not amorphous material. It does etch more like polycrystalline material due to the high density of defects. It is fortunate that the Si grown in the recess corner (110) does etch at a slightly higher rate than the material grown on the (100) surface (See Fig.5).

Reducing and eliminating the corner defect (micro twins) is usually accomplished by increasing the etch time by a few seconds depending on the severity of the micro-twins. Too much etching and a notch will form next to the gate which is undesirable. Carefully optimizing deposit and etch time results in a filled recess with no micro-twins and no notching from excessive etching.

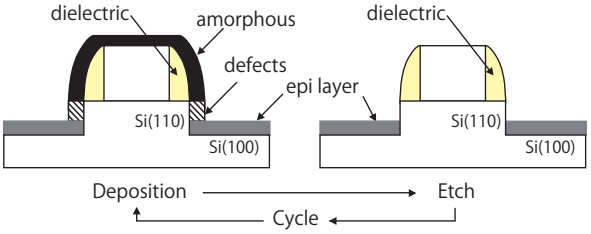

Fig. 5: Scheme of cyclical deposition and etch

4.1.3 Gas phase nucleation

CDE not only is beneficial for removing the defective growth on the Si (110) plane but it is also very beneficial in removing gas phase defects from the growth of Si:C films with TF-2 [6]. TF-2 precursor is a high order silane which is high reactive molecule with low activation energies. They tend to polymerize and form higher order chains which are deposited as particles. These particles nucleate at/near the initial growth interface. **Fig.6 (a)** shows a 25nm thickness one-step SiCP growth with TF-2, mono-methylsilane and phosphine using a growth rate of 35nm/min at 550 ºC. Gas phase particles are observed on the as grown SiCP interface by AFM scans (scan area; 10 µm x 10 µm). On the other hand, **Fig. 6 (b)** depicts a particle-free surface (RMS : 0.33 nm) of 25 nm thick SiCP epitaxy done by using a CDE process. By carefully optimizing the growth and etch portion of the CDE process recipe both micro-twins and gas phase particles are eliminated from the growth and a defect free film can be obtained.

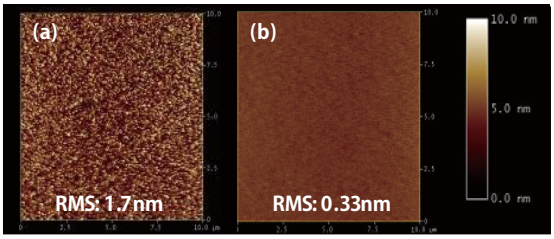

Fig. 6: AFM scans of (a) one-step SiCP film with TF-2 (not optimized process for gas phase particle) and (b) CDE SiCP film with TF-2 (optimized process)

4.2 SiCP film growth with TF-2

Si:C growth with high carbon concentration (C > 2%) has to overcome three distinct difficulties. The first is the large lattice mismatch (~40%) between silicon and carbon atoms. The incorporation of carbon atoms generate a large local strain on its nearby atoms, causing each individual carbon atom to be highly unstable in a substitutional site potentially leaving large concentrations of interstitial carbon atoms. The second difficulty is that unlike SiGe which is miscible, Si:C has a stable phase, silicon-carbide which exist between diamond and silicon. This stable phase will cause precipitates to occur for larger fractions of carbon in the Si:C film. The third difficulty is the low solid solubility of carbon in silicon, of $3.5x10^{17}$ atoms cm^{-3} and with extrapolation at 700ºC suggesting a value of approximately $5x10^{12}$ atoms cm^{-3}. For SiP deposition the incorporation of large amounts of phosphorus in the layers is also difficult. This is due to the well-known surface segregation effect of phosphorus atoms. (i.e. the majority of phosphorus atoms which land on the surface will "segregate" ; ride back to the growth surface instead of being incorporated into the layer). This effect will also inhibit the growth rate due to the large number of stable phosphorus-hydrogen bonds on the surface. The use of the high order silane TF-2 can overcome these difficulties due to its high-growth at low temperatures. The growth at low temperatures allows for the supersaturation of carbon atoms in silicon. The growth of metastable layers with such high C is possible during growth because the surface solubility rather than the bulk solubility plays a more important role. Used in conjunction with a high-growth rate (35nm/min at 550ºC) this will "freeze" out both the phosphorus and the carbon atoms into subsitutional sites, thus mitigating the surface segregation effect of phosphorus and trapping carbon atoms into its unfavorable configuration in the substitutional site. Lowering the deposition temperature increases the amount of substitutional C. Ideally, the temperature is lowered until the total C as measured by SIMS, matches substitutional C as measured by XRD. The graph with TF-2 chemistry deposited using RPCVD 550ºC CDE process (XRD results in **Fig.7**) demonstrates up to 2.3% C can be put into substitutional sites.

Due to the issues of Si:C precipitates, defective growth on the sidewall (110) surface, and gas phase nucleation particulates brought on by the use of TF-2, CDE of defective areas is required as

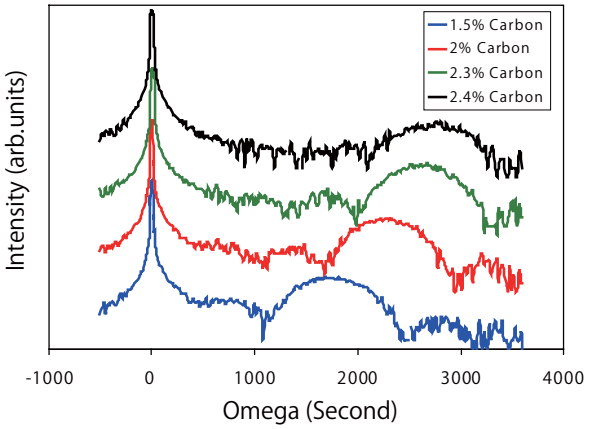

Fig. 7: XRD results of SiCP film with TF-2: up to 2.3% C substitutional profiles are obtained

described in section 4.1. In our process we use an HCl-based etchant at 550°C for the removal of the aforementioned defects and particulate We have found that a deposition of 4nm followed by an etch of 2nm was found to be optimal in terms of minimizing the etch required to remove defective areas along the sidewall (110) surface and eliminating gas phase particles which occur with the use of TF-2, while maximizing the growth along the (100) orientation. This process has demonstrated the ability to fill small recesses down to 40nm in length with SiCP of carbon concentrations in excess of 2% and phosphorus concentration of $5x10^{20}$ atoms cm^{-3} in the layers (SIMS profile in **Fig.8**).

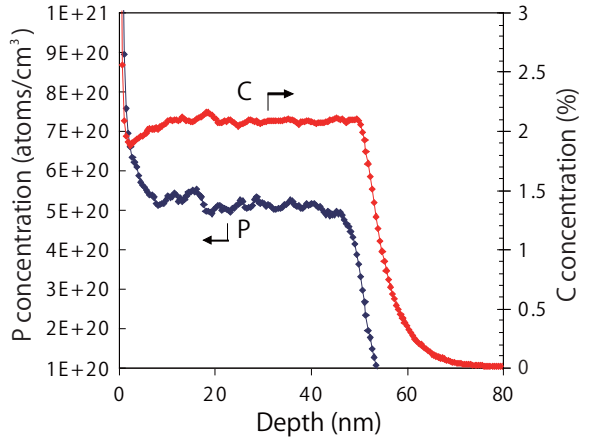

Fig. 8 SIMS profile of SiCP film with TF-2

4.3: SiGeB film growth with TF-2

The main focus is to deposit SiGe epitaxial film with high substitutional Ge concentration (>40%) to transfer significant strain to the channel area. Due to the lattice constant mismatch between Si and Ge atoms (4.2%), misfit dislocations and stacking faults from relaxation are formed in high-concentration SiGe film which exceeds the metastable thickness [7]. To achieve fully-strained SiGe for Ge percentages at 40% and higher, with thickness in excess of 50 nm, the deposition temperature needs to be lowered to 500°C and below [8]. Therefore, we use TF-2 in conjunction with GeH_4 as the Ge source to deposit SiGe epitaxial films with high Ge concentrations (>40%) and high growth rates (>10 nm/min) at 500°C.

The goal of SiGeB film was to develop selective B-doped SiGe process with 40% Ge concentration and higher, however due to the current hardware limitations at the time of this report, the highest Ge% currently achieved in our tool is around 38% with boron concentration $2x10^{20}$ atoms cm^{-3} (XRD results in **Fig.9**) [9]. Nevertheless, the high growth rates and low temperatures enabled by TF-2 provides a process window using RPCVD that is conducive for the selective epitaxial growth of high Ge percentage up to 60% and boron concentration of $2-8x10^{20}$ atoms cm^{-3} with sufficient epitaxial thicknesses (>60nm) required for SiGe stressor films. Reasonable selective epitaxial growth rates are obtained with the isothermal 500°C CDE process that are compatible with high volume manufacturing.

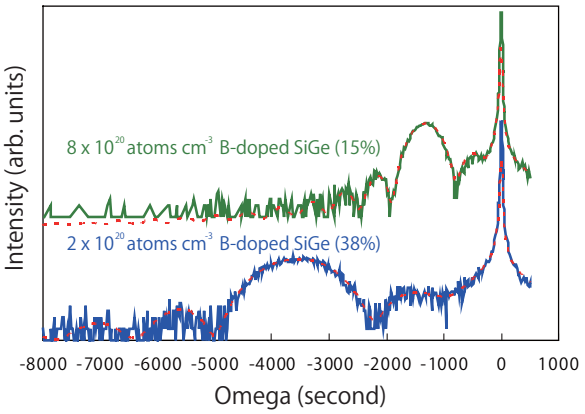

Fig. 9: XRD results of SiGeB film with TF-2: up to 38% Ge substitutional profiles are obtained

5. Conclusion

In this report, our challenges are described for low temperature silicon-based epitaxial process. For moisture challenges of low temperature, our purification system realizes extremely high purity gas delivery to RPCVD tool. For low thermal budget H_2 prebake, we optimized temperature to 775°C. For breakthrough to both low temperature process and high volume manufacturing, novel processes with TF-2 unique silicon precursor are optimized using CDE process with solutions of selective, defective and gas particle issues. Moreover, SiCP of carbon concentrations in excess of 2% and

phosphorus concentration of $5x10^{20}$ atoms cm^{-3} for nMOS is realized at 550°C. SiGeB of germanium concentration around 38% and boron concentration $2x10^{20}$ atoms cm^{-3} for pMOS is achieved at 500°C. We conclude that TF-2 is useful precursor to realize highly substitution and doped film of silicon-based epitaxial at low temperature (<600°C) for Source/Drain formation of CMOS device for 22nm node and beyond.

Acknowledgment

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